IN THE CLAIMS

1. (original) A method of generating a deep N-well pattern for an integrated circuit design, said method comprising:

specifying a tile comprising a first layer wherein said first layer comprises a first layer element for a deep N-well pattern;

arranging multiple instances of said tile to create a tile array covering a portion of said integrated circuit design; and

merging said tiles to produce a deep N-well pattern.

2. (original) The method of Claim 1, wherein said tile further comprises a second layer, wherein said second layer comprises a second layer element.

3. (original) The method of Claim 2, wherein said first layer element is identical in shape to said second layer element.

4. (original) The method of Claim 3, wherein said first layer element is disposed rotated with respect to said second layer element.

5. (original) The method of Claim 1, further comprising editing said tile array.

Claims 6-7 (canceled) (restriction)

8. (original) The method of Claim 2, further comprising flattening said first layer and said second layer.

Claims 9-24 (canceled) (restriction)